PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Charles A. MILLER

Application No: 09/819,181

Filed: March 27, 2001

For: METHOD FOR FABRICATING AN IC INTERCONNECT SYSTEM INCLUDING AN IN-STREET INTEGRATED CIRCUIT WAFER VIA

Art Unit: 3729

Examiner: Rick K. Chang

REPLY TO THE OFFICE ACTION MAILED 02/19/2002

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Further examination and consideration of this application are requested in view of the following Amendments and Remarks.

AMENDMENTS

The Title:

Please amend the title to read as follows:

METHOD FOR FABRICATING AN IC INTERCONNECT SYSTEM INCLUDING AN IN-STREET INTEGRATED CIRCUIT WAFER VIA

In the Claims:

Claims 13-18, rewrite as follows:

13. (Amended) A method for fabricating an interconnect system for providing a signal path to a first circuit node of an integrated circuit (IC) formed within and on a portion of a semiconductor wafer having horizontal upper and lower surfaces, the method comprising the steps of:

a. forming a hole extending vertically through an area of the semiconductor wafer adjacent to the portion of the wafer containing the IC, and

b. placing a first conductive material in the hole, the first conductive material vertically extending through the hole, and

c. conductively linking the first conductive material to the first circuit node.